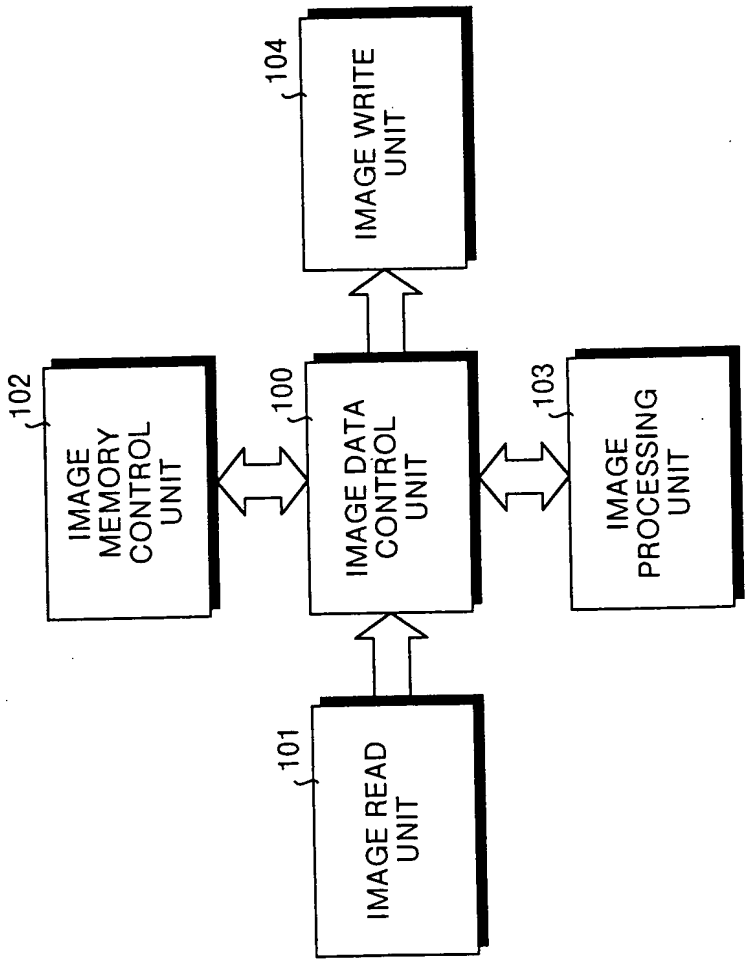
FIG.1


104
IMAGE WRITE UNIT
102
IMAGE MEMORY CONTROL UNIT
100
IMAGE DATA CONTROL UNIT
103
IMAGE PROCESSING UNIT
101
IMAGE READ UNIT

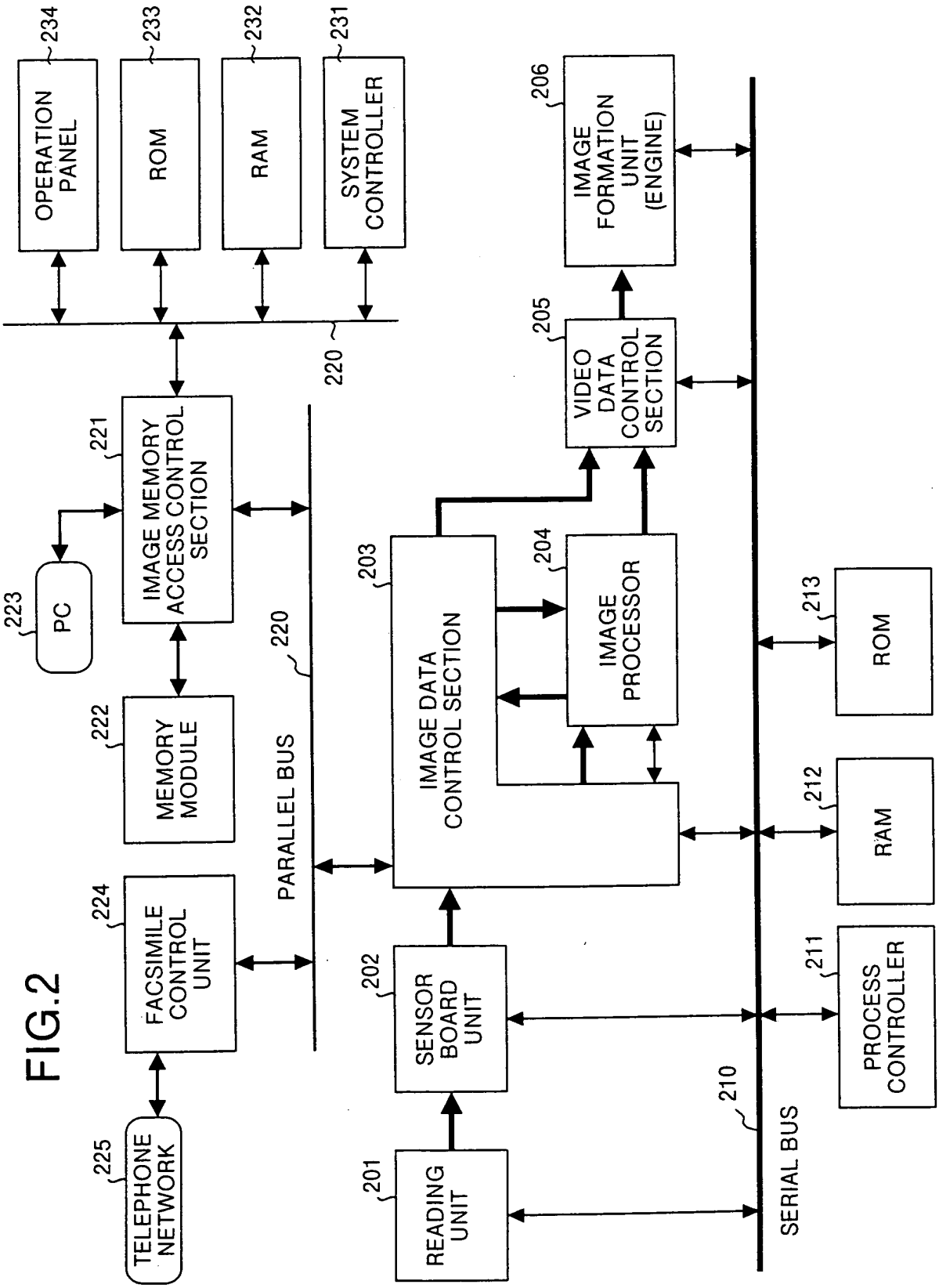

OPERATION PANEL
234
ROM
233
RAM
232
SYSTEM CONTROLLER
231
220
IMAGE FORMATION UNIT (ENGINE)
206
VIDEO DATA CONTROL SECTION
205
IMAGE MEMORY ACCESS CONTROL SECTION
221
PC
223
MEMORY MODULE
222
PARALLEL BUS
220
IMAGE DATA CONTROL SECTION
203
IMAGE PROCESSOR
204
ROM
213
RAM
212
FACSIMILE CONTROL UNIT
224
SENSOR BOARD UNIT
202
PROCESS CONTROLLER
211
TELEPHONE NETWORK
225
READING UNIT
201
SERIAL BUS
210

FIG.2

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FIG.3

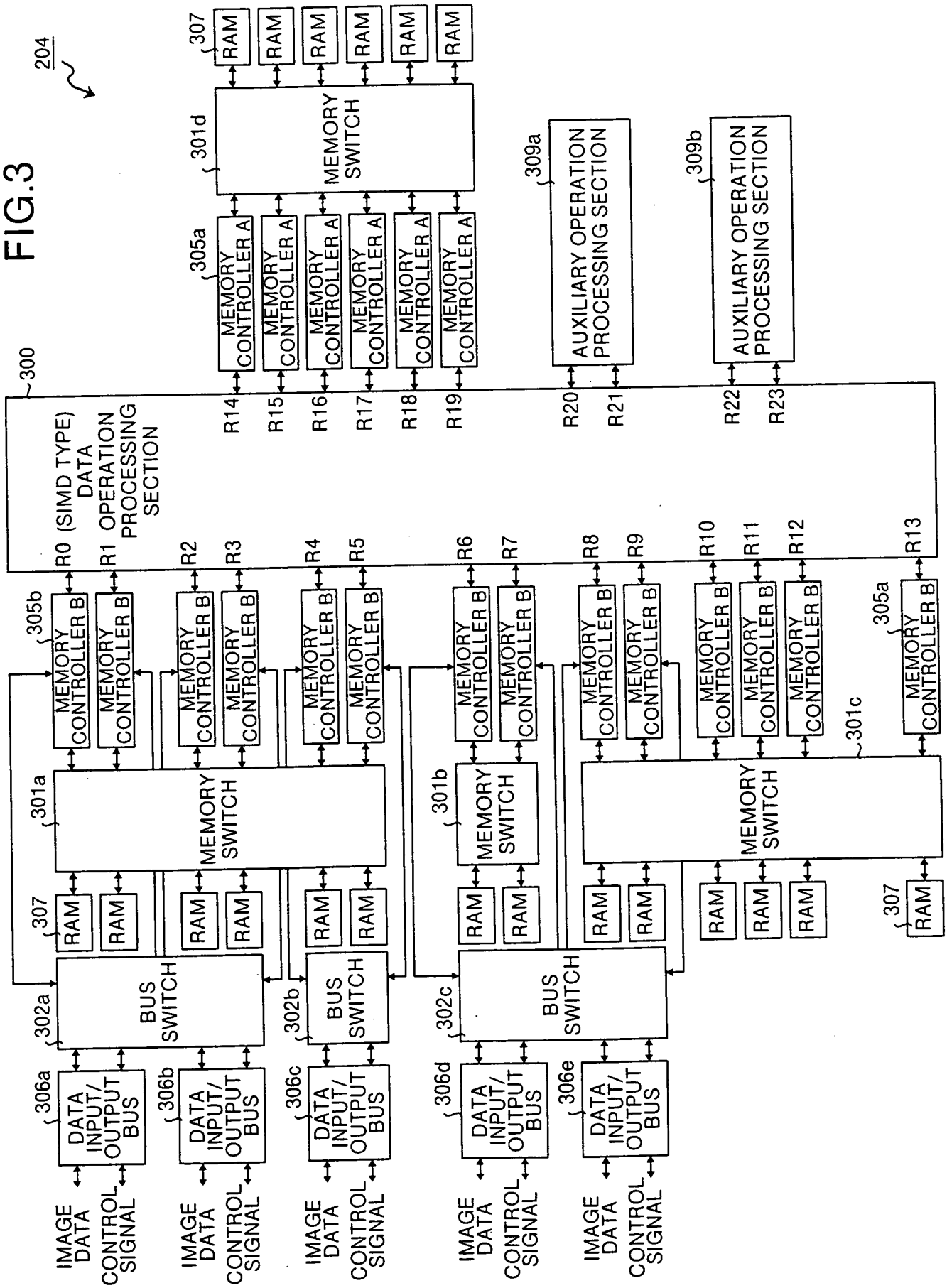
204
300
(SIMD TYPE) DATA OPERATION PROCESSING SECTION
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
301a
301b
301c
301d
MEMORY SWITCH
302a
302b
302c
BUS SWITCH
305a
305b
MEMORY CONTROLLER A
MEMORY CONTROLLER B
307
RAM
309a
309b
AUXILIARY OPERATION PROCESSING SECTION
306a
306b
306c
306d
306e
DATA INPUT/OUTPUT BUS
IMAGE DATA
CONTROL SIGNAL

FIG.4

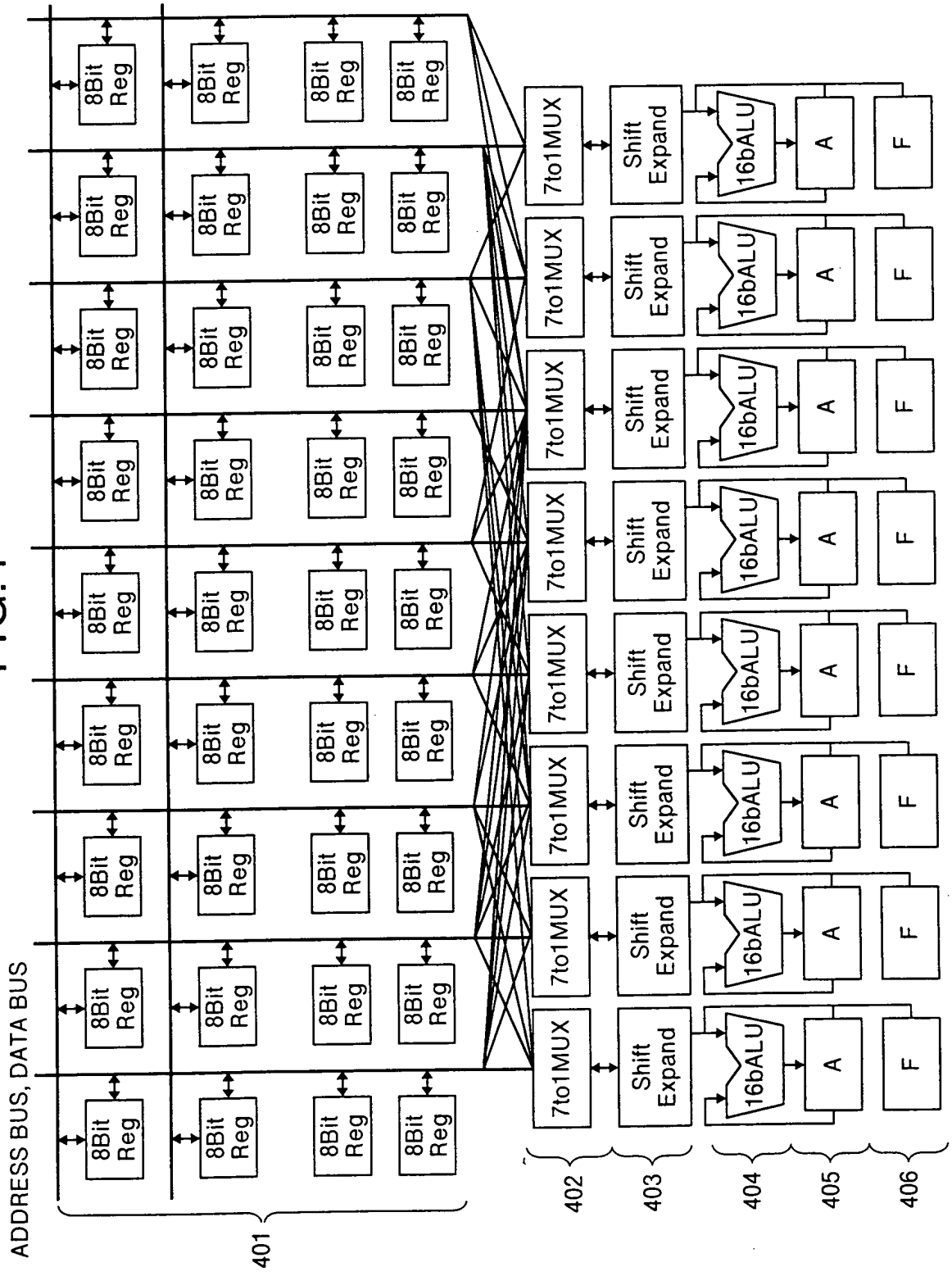
ADDRESS BUS, DATA BUS
8Bit Reg
7to1MUX
Shift Expand
16bALU
A
F
401
402
403
404
405
406

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FIG.5

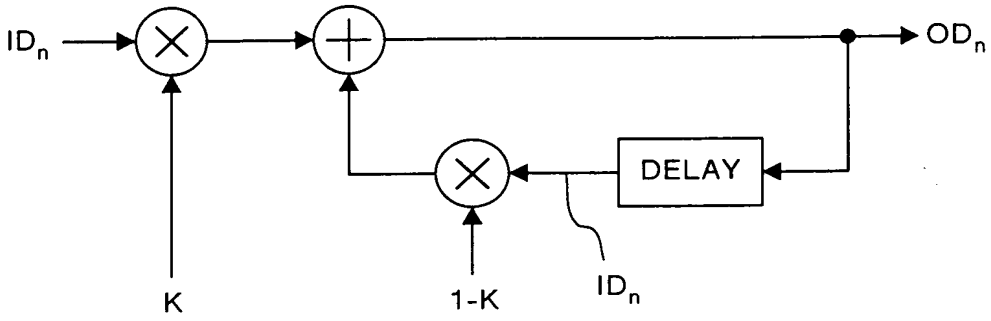


FIG.6

MODE	REGISTER 0 (R0)	REGISTER 1 (R1)	REGISTER 2 (R2)	REGISTER 3 (R3)	REGISTER 4 (R4)	REGISTER 5 (R5)
A	TWO RAMS/TWO RAMS NORMAL/TOGGLE		ONE RAM/TWO RAMS NORMAL/TOGGLE		ONE RAM/TWO RAMS NORMAL/TOGGLE	
B	TWO RAMS NORMAL	ONE RAM NORMAL	—	ONE RAM NORMAL	ONE RAM/TWO RAMS NORMAL/TOGGLE	
C	TWO RAMS TOGGLE	—	—	—	ONE RAM/TWO RAMS NORMAL/TOGGLE	
D	THREE RAMS NORMAL	—	ONE RAM/TWO RAMS NORMAL/TOGGLE		ONE RAM NORMAL	—
E	THREE RAMS NORMAL	ONE RAM NORMAL	—	ONE RAM NORMAL	ONE RAM NORMAL	—
F	THREE RAMS NORMAL	—	THREE RAMS NORMAL	—	—	—
G	THREE RAMS TOGGLE	—	—	—	—	—

FIG.7

REGISTER 0,2,4 (R0,R2,R4)	REGISTER 1,3,5 (R1,R3,R5)
ONE RAM NORMAL	ONE RAM NORMAL
ONE RAM TOGGLE	—
TWO RAMS NORMAL	—

FIG.8

MODE	REGISTER 6 (R6)	REGISTER 7 (R7)
H	ONE RAM NORMAL	ONE RAM NORMAL
I	ONE RAM TOGGLE	—
J	TWO RAMS NORMAL	—

FIG.9

MODE	INPUT/OUTPUT OF REGISTER 0 (R0)	INPUT/OUTPUT OF REGISTER 1 (R1)	INPUT/OUTPUT OF REGISTER 2 (R2)	INPUT/OUTPUT OF REGISTER 3 (R3)
K	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 0	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 0	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 1	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 1
L	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 0	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 0	16 BITS OF DATA INPUT/ OUTPUT BUS 1	—
M	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 0	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 0	—	16 BITS OF DATA INPUT/ OUTPUT BUS 1
N	16 BITS OF DATA INPUT/ OUTPUT BUS 0	—	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 1	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 1
O	16 BITS OF DATA INPUT/ OUTPUT BUS 0	—	16 BITS OF DATA INPUT/ OUTPUT BUS 1	—
P	16 BITS OF DATA INPUT/ OUTPUT BUS 0	—	—	16 BITS OF DATA INPUT/ OUTPUT BUS 1
Q	—	16 BITS OF DATA INPUT/ OUTPUT BUS 0	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 1	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 1
R	—	16 BITS OF DATA INPUT/ OUTPUT BUS 0	16 BITS OF DATA INPUT/ OUTPUT BUS 1	—
S	—	16 BITS OF DATA INPUT/ OUTPUT BUS 0	—	16 BITS OF DATA INPUT/ OUTPUT BUS 1
T	32 BITS OF DATA INPUT/ OUTPUT BUSES 0 AND 1	—	—	—
U	—	32 BITS OF DATA INPUT/ OUTPUT BUSES 0 AND 1	—	—

FIG.10

MODE	INPUT/OUTPUT OF REGISTER 4 (R4)	INPUT/OUTPUT OF REGISTER 5 (R5)
V	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 2	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 2
W	16 BITS OF DATA INPUT/ OUTPUT BUS 2	—
X	—	16 BITS OF DATA INPUT OUTPUT BUS 2

FIG.11

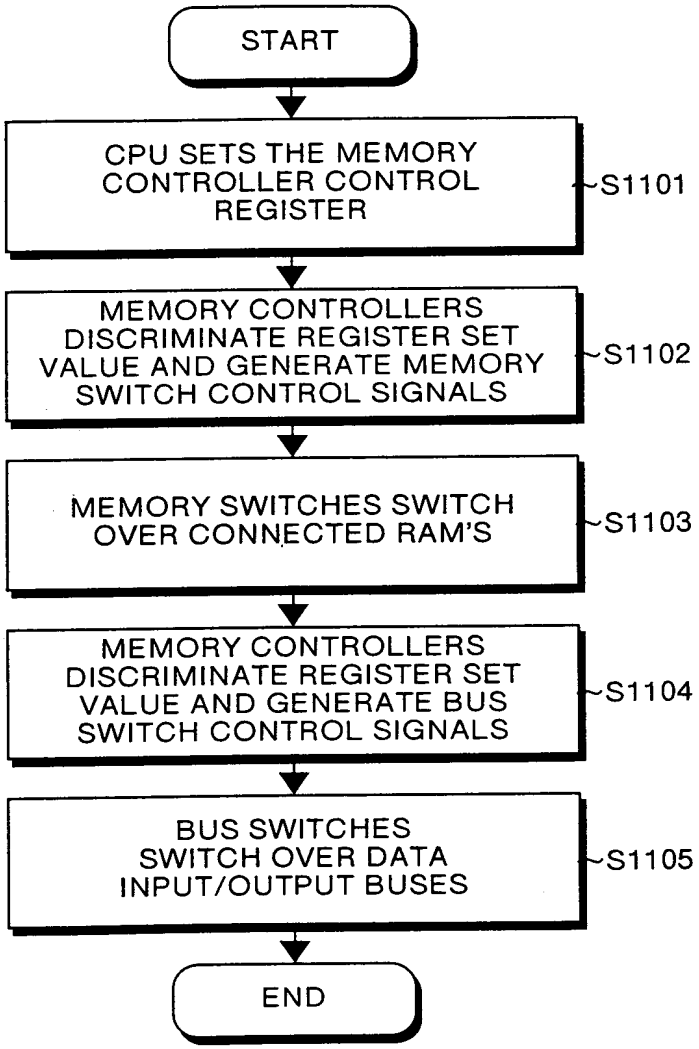

START
CPU SETS THE MEMORY CONTROLLER CONTROL REGISTER
S1101
MEMORY CONTROLLERS DISCRIMINATE REGISTER SET VALUE AND GENERATE MEMORY SWITCH CONTROL SIGNALS
S1102
MEMORY SWITCHES SWITCH OVER CONNECTED RAM'S
S1103
MEMORY CONTROLLERS DISCRIMINATE REGISTER SET VALUE AND GENERATE BUS SWITCH CONTROL SIGNALS
S1104
BUS SWITCHES SWITCH OVER DATA INPUT/OUTPUT BUSES
S1105
END

FIG.12

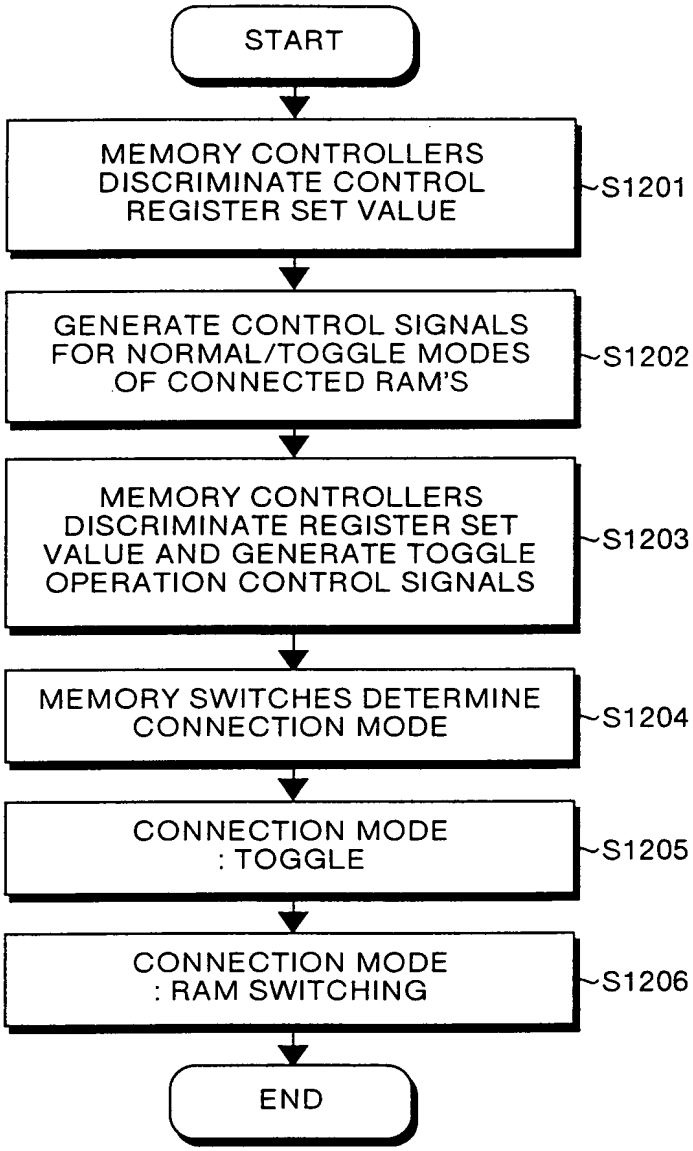
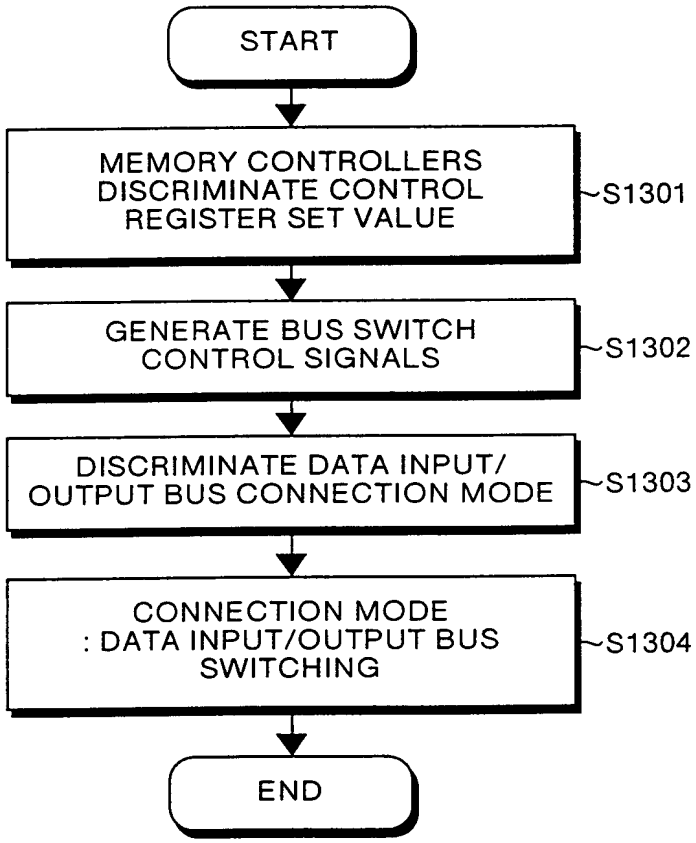

START
MEMORY CONTROLLERS DISCRIMINATE CONTROL REGISTER SET VALUE
S1201
GENERATE CONTROL SIGNALS FOR NORMAL/TOGGLE MODES OF CONNECTED RAM'S
S1202
MEMORY CONTROLLERS DISCRIMINATE REGISTER SET VALUE AND GENERATE TOGGLE OPERATION CONTROL SIGNALS
S1203
MEMORY SWITCHES DETERMINE CONNECTION MODE
S1204
CONNECTION MODE : TOGGLE
S1205
CONNECTION MODE : RAM SWITCHING
S1206
END

FIG.13


START
MEMORY CONTROLLERS DISCRIMINATE CONTROL REGISTER SET VALUE
S1301
GENERATE BUS SWITCH CONTROL SIGNALS
S1302
DISCRIMINATE DATA INPUT/ OUTPUT BUS CONNECTION MODE
S1303
CONNECTION MODE : DATA INPUT/OUTPUT BUS SWITCHING
S1304
END